

# A COMPARATIVE ANALYSIS OF LEAKAGE REDUCTION TECHNIQUES IN NANOSCALE CMOS ARITHMETIC CIRCUITS

Frank Anthony Hurtado and Eugene John  
Department of Electrical and Computer Engineering  
The University of Texas at San Antonio  
frankhurtado91@gmail.com

## Abstract

In this undergraduate research, various leakage reduction techniques such as power gating, multiple thresholded voltage and high k-dielectric are investigated. These techniques and their effectiveness are explored by experimentation on various nanoscale CMOS arithmetic circuits. These circuits include full adders, combinational multipliers, Booth multiplier and divider circuits. Using Predictive Technology Models (PTM) of CMOS transistors in the 32, 45, 65 and 90 nanometer technology nodes, threshold voltage and power gating is applied to the arithmetic circuits to experiment the efficiency and viability of such method and their limitations. Power gating with high-K transistors is then investigated to analyze the effects of such a combination. Finally, the results are compared and the effectiveness of the various leakage reduction techniques is analyzed. Threshold voltage change proved to have the most impact on performance and less of an impact on leakage reduction while power gating offered no significant performance drop and the highest impact on leakage power reduction.

## 1. Introduction

Technology scaling and the large number of transistors on an integrated circuit has resulted in several design challenges, including increased leakage power, increased wire capacitance, increased resistance due to temperature, and an increase in soft error rate [1]. As technology progresses and allows for smaller feature sizes, the nature of power consumption in CMOS circuits changes. Smaller channel lengths and supply voltages ultimately reduce dynamic power consumption per transistor and permit faster transistor operation. While desirable, transistor scaling also comes with a drawback; the smaller gate oxide thickness and the lower threshold voltage substantially increase the transistor leakage power consumption. As a result, as transistors become smaller and smaller, the leakage power consumption grows and is now a significant problem that has to be addressed [2].

## 2. Methodology

Simulation of the various arithmetic circuits was accomplished with HSPICE circuit simulator and by using the Predictive Technology Models (PTM) of CMOS transistors from the Arizona State University [3]. The 32, 45, 65 and 90 nm channel length models were used to investigate the leakage trends within the modeled circuits. Keeping some parameters constant between the circuits ensured the reliability of the collected information. Supply voltage was kept at 1 volt, channel widths at two times the channel length, input waveforms at same frequency and clock signals maintained the same period throughout every test to guarantee that the leakage power consumption test results only showed the effects of the method being tested. Functionality of the circuits was tested and dynamic power consumption simulations were performed. Since the transistor count of each respective circuit did not vary between tests, the well-known

correlation between transistor count and dynamic power in conjunction with output waveforms was a key assurance to validating the results.

### 3. Full Adder

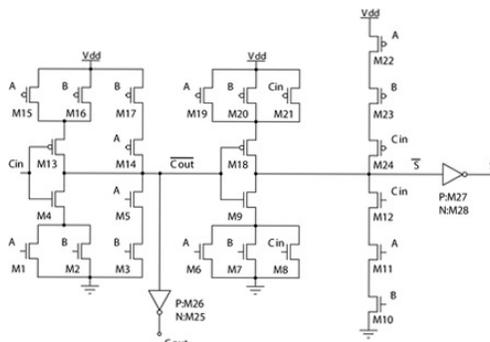


Fig 1: Full adder transistor circuit used for HSPICE simulation [4]

#### 3.1 Dynamic and Leakage Power Consumption

As mentioned earlier, dynamic power consumption of the full adder circuit showed that as feature size increased, so did the dynamic power consumption. Furthermore, as feature size increased, gate thicknesses also increased and leakage power decreased. These trends can be observed below in Fig. 2. In circuits with low transistor count, dynamic power is more significant than leakage power in the circuit's total power consumption.

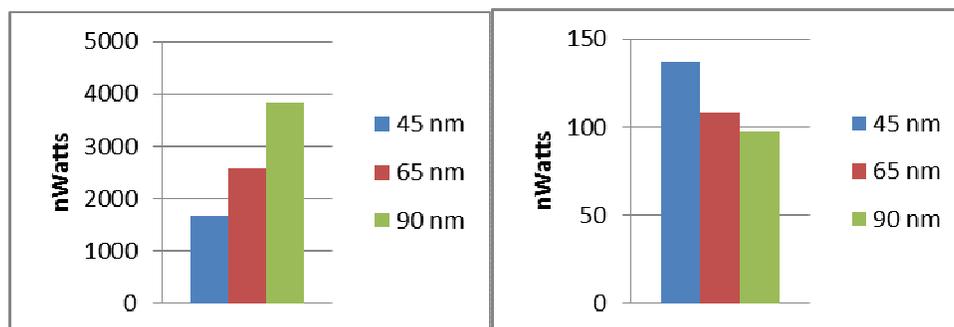


Fig. 2: Dynamic (left) and leakage (right) power of the full adder circuit

#### 3.2 Threshold Voltage

CMOS circuits follow the same trend when the transistor's threshold voltage is varied. By increasing/decreasing the threshold voltage by 25%, dynamic power consumption increases/decreases correspondingly. Most notably, the effect on leakage power consumption can be observed in Fig. 3. Decreasing the threshold voltage by 25% increases the circuit leakage power by 6X. This is due to the decreased amount of voltage needed to turn the transistor on, but increasing the threshold voltage by 25% decreases leakage power by 85%. When lower power consumption from a circuit in standby is needed as in the case of conserving battery power, increasing the threshold voltage will significantly reduce the amount of leakage power.

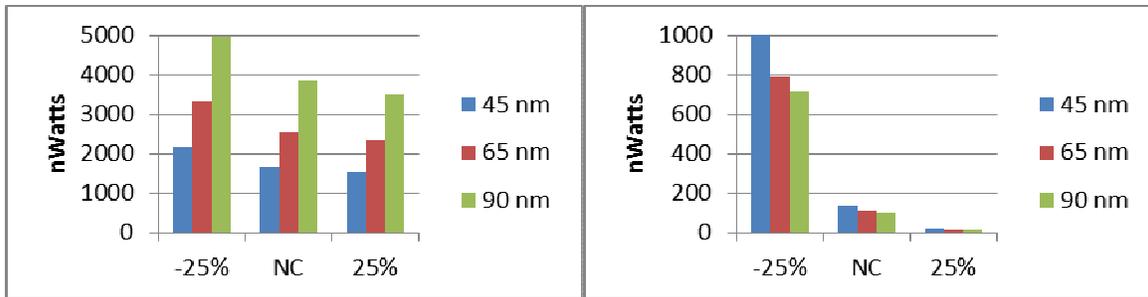


Fig. 3: Threshold voltage effects on dynamic (left) and leakage power (right) in full adder circuit, where NC means no change.

### 3.3 Power Gating and High-K Power Gating

Even though increasing a transistor's threshold voltage decreases leakage current to desirable amounts, output delays also increase and when circuits expand, these delays accumulate and could present undesirable performance. Turning off sleep transistors when the circuit is not in use, virtually disconnects the gated circuit from the power rails and the circuit leakage power is essentially composed of only the sleep transistors' leakage power. Results from the 45 nm full adder simulations are shown in Figure 4, and other results show similar trends. Power gating alone decreased leakage power by 85%. This decrease was the same as an increase in threshold voltage but output delays did not increase.

Using High-k materials in the gates of the sleep transistors proved more effective than power gating alone. The use of High-k technology allows transistor gate thickness to increase while maintaining optimum channel formation. This allowed an extra 99% decrease than power gating without High-k sleep transistors. From Fig 4, High-k power gating is almost unperceivable; this value is 0.14 nW and is the most effective leakage power reducing technique.

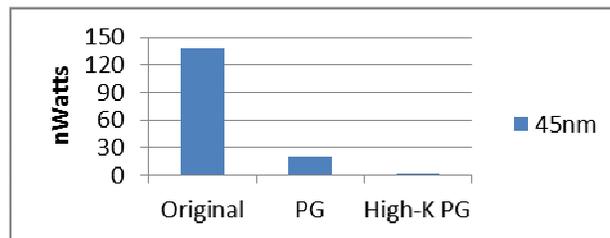


Fig. 4: Power gating and High-K power gating effects on full adder circuit

## 4. Array Multiplier

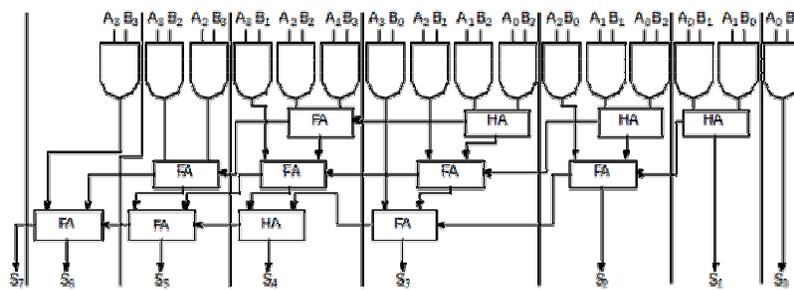


Fig. 5: Circuit design of 4x4 bit array multiplier simulated in HSPICE [5]

#### 4.1 Dynamic and Leakage Power Consumption

As the array multiplier circuit grows to accommodate longer word lengths, the transistor count of the circuit increases in an exponential fashion. As seen in Fig. 6, bigger circuits have larger dynamic power consumption. More transistors also mean a higher leakage power. The leakage power increases at a slower rate than dynamic power but becomes significant enough to become an overall circuit performance degrader. Increasing the multiplier size from a 4x4 bit multiplier to a 32x32 bit multiplier increases the leakage by a factor of 100 (100X).

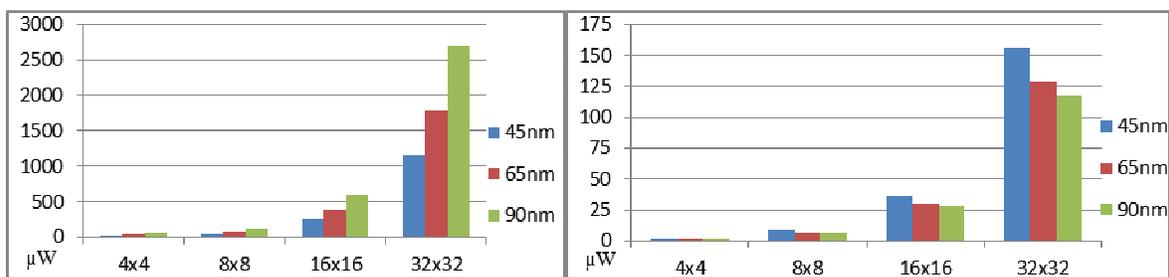


Fig. 6: Dynamic (left) and leakage (right) power consumption of combinational multiplier

#### 4.2 Threshold Voltage

Decreasing the threshold voltage of the combinational multiplier also decreased its performance. Even though leakage power was reduced by 84%, delay times grew by an average of 42% across each multiplier circuit. Only the 4x4 bit multiplier is shown because the rest of the multiplier circuits display very similar results as the ones shown below.

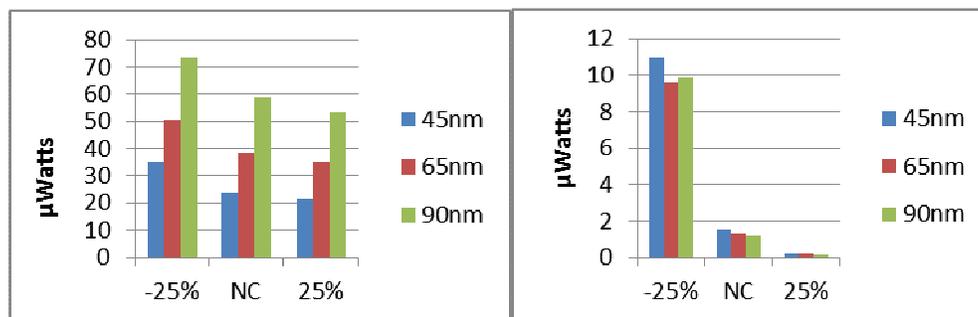


Fig. 7: Threshold voltage effect on dynamic (left) and leakage (right) power consumption of a 4 bit x4 bit combinational multiplier

#### 4.3 Power Gating and High-K Power Gating

Due to the limitations of coarse-grain power gating, a trade-off between performance and leakage power has to be chosen. When the circuit in isolation from the power rails is too large, the sleep transistors have to increase in size to maintain the current needed to not lose performance. When this is done, the size of the sleep transistors is big enough to not show any effect on leakage power reduction and in some cases a higher leakage power can be observed. [6] The 4x4 bit multiplier was the circuit that benefited the most from power gating with a transistor count of 432 transistors. Power gating alone decreased the leakage power consumption by 84% while using High-k sleep transistors decreased leakage power by an additional 99.5%. Leakage current was decreased from the microwatt range to the nanowatt range at an average of 1.6 nW of leakage power. Larger circuits meant sleep transistors needed to be bigger to keep current high

enough in order for output delay increases to be unperceivable. This effect is broadened as feature size increases since larger transistors also consume larger amounts of power than smaller transistors.

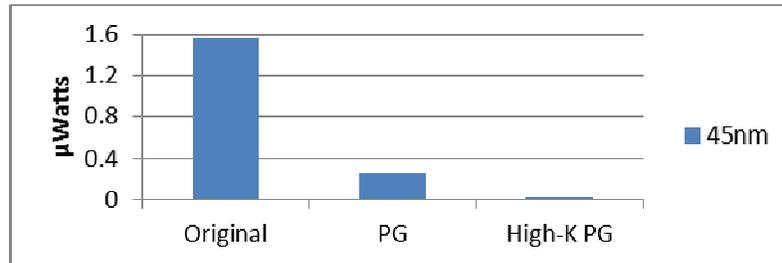


Fig. 8: Power gating and High-k power gating effects on 4x4 bit combinational multiplier

## 5. Booth Multiplier

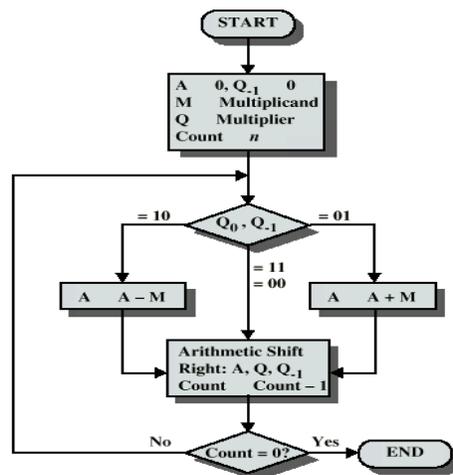


Fig. 9: Booth multiplier logic diagram simulated in HSPICE [7]

### 5.1 Dynamic and Leakage Power

Memory is a significant part in the construction of the Booth's multiplier circuit. Consequently, leakage power starts to reach dynamic power levels. In addition some of the registers are only used once to initialize values and then remain inactive throughout the calculation process [8]. These memory modules use a considerable amount of transistors which, in this case, makes leakage power more significant in the total power dissipation of the circuit.

Likewise, leakage power decreases as feature size increases as observed below. The PTM may not be perfect models but output waveform data proved correct functionality of the Booth multiplier circuit. Nonetheless, the global tests showed the expected trends in power dissipation.

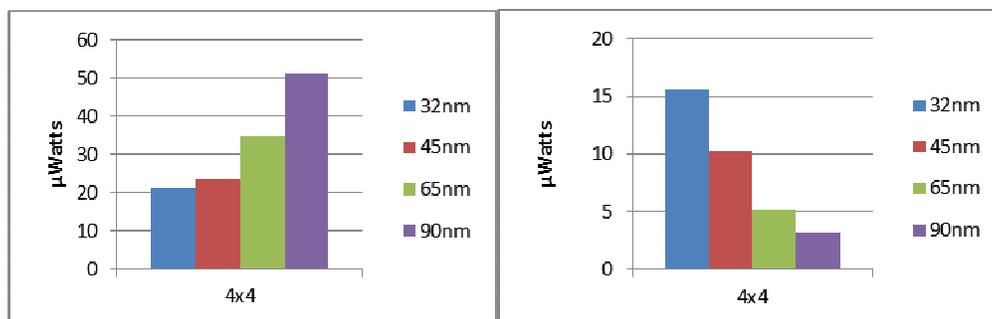


Fig. 10: Dynamic (left) and leakage (right) power of 4x4 bit Booth multiplier

## 5.2 Threshold Voltage

Increasing the threshold voltage by 25% resulted in a 60% decrease in leakage power. This is much less of an effect for this sequential circuit than the combinational circuit. Doing so did not affect the performance of the circuit. The output was well within the allotted clock period and correct values were present at the fourth clock period necessary for reading the product of a 4x4 bit Booth multiplier. There is much more flexibility in sequential circuits in setting a desired output delay and making adjustments to the circuit within the set clock period. Even though this multiplier has a longer delay between input and output waveforms, the Booth multiplier has greater functionality as it also allows the multiplication of signed words.

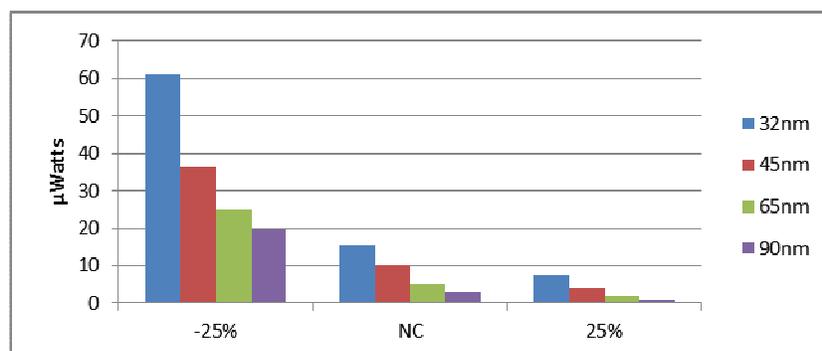


Fig. 11: Threshold voltage effects on leakage power of 4x4 bit Booth multiplier

## 5.3 Power Gating and High-K Power Gating

The 32 nm transistor PTM models are only available with High-K gate materials but high performance and low power models exist. The power gating models use high performance transistors throughout the circuit while the High-k power gating model uses low power transistors for the sleep transistors. Furthermore, High-k models only extend up to the 45 nm technology. Even when High-k transistors make up a circuit, power gating is still a viable option as it lowers leakage current by 58.38%. Using lower power transistors in the sleep transistors further lowers leakage current by an additional 71.75%. Power gating alone brings the leakage power to power levels similar to the combinational multiplier but with the addition of an increased functionality, this makes power gating a needed adjustment. Using low power transistors in the sleep transistors brings the leakage power to lower levels. This is a significant improvement without a loss of performance provided that the output is read and stored elsewhere.

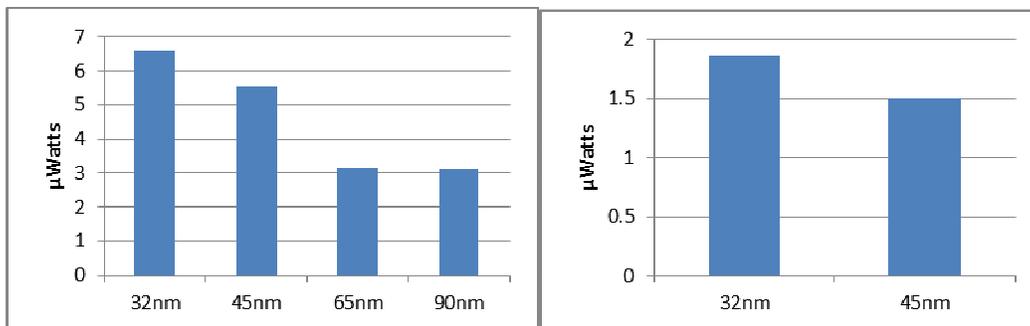


Fig. 12: Power gating (left) and High-k power gating (right) effects on 4x4 bit booth multiplier

## 6. Divider

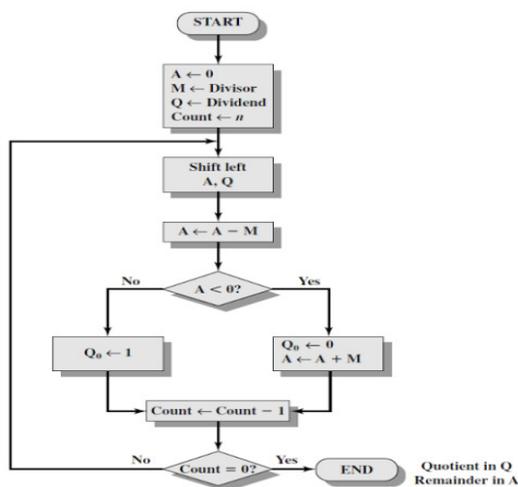


Fig. 13: Divider logic algorithm simulated in HSPICE [7]

### 6.1 Dynamic and Leakage Power Consumption

The divider circuit shows similar characteristics as the Booth multiplier. Consisting of memory registers, the leakage power is more significant to the total power consumption of the circuit.

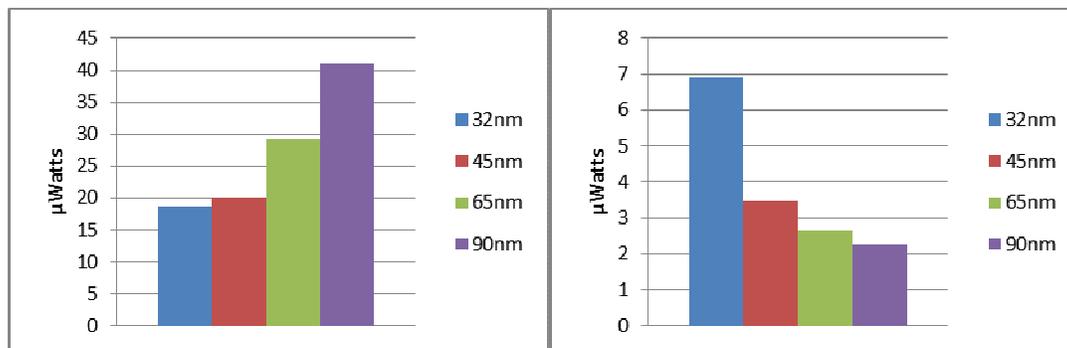


Fig. 14: Dynamic (left) and leakage (right) power consumption of divider circuit

## 6.2 Threshold Voltage

Increasing the threshold voltage did not have an effect on the output delay of the divider circuit. The calculations flowed well within the four clock cycles needed for the output to be read correctly. Increasing the threshold voltage decreased leakage power by 74%.

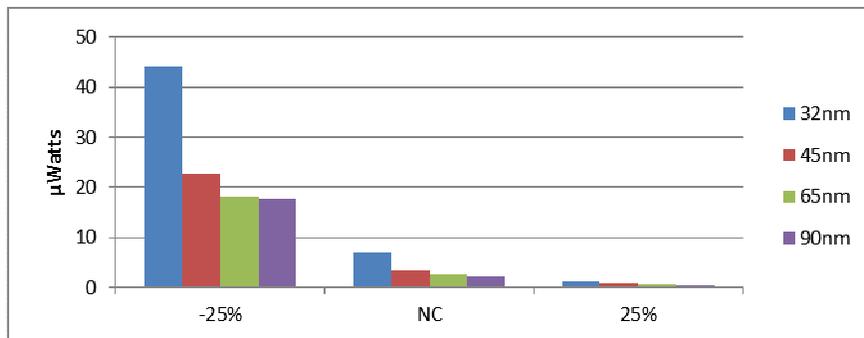


Fig. 15: Threshold voltage effects on divider circuit

## 6.3 Power Gating and High-K Power Gating

Power gating significantly reduced the leakage power consumption of the divider circuit. On average power gating reduced leakage power by 56.34%. Further using low power models for the sleep transistors reduced leakage power an additional 93.98%.

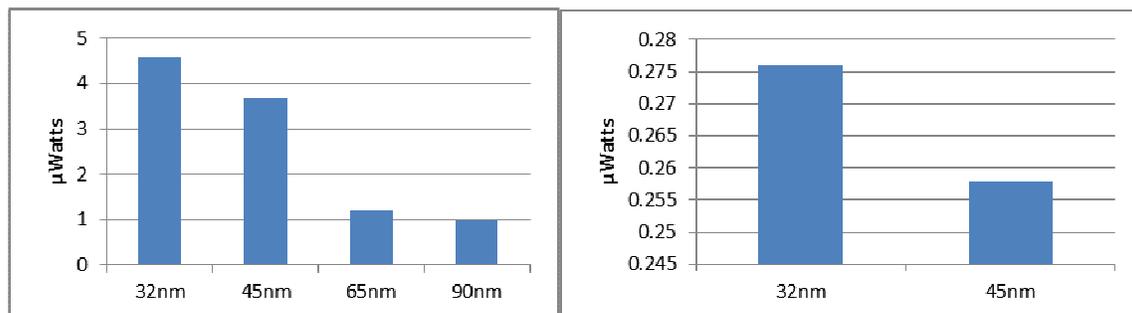


Fig. 16: Power gating (left) and High-k power gating (right) effects on divider circuit

## 7. Conclusion

Power gating is the most effective technique in reducing leakage power in combinational circuits. Choosing the correct sleep transistor size allows the circuit to perform without incrementing output delays as does increasing threshold voltage. This is beneficial since these types of circuits are parts of a bigger chip and keeping delay low increases overall chip performance. Using High-k sleep transistors proved to be the best method to reduce leakage power in both sequential and combinational circuits. Sequential methods benefit from each of the methods and choosing the most adequate method comes down to circuit complexity and cost. Increasing the threshold voltage provides a significant amount of leakage power reduction and is the most cost-effective solution. If an even lower leakage power is required, power gating and High-k power gating are the most viable solutions with substantial power reduction effects.

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## 8. References

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